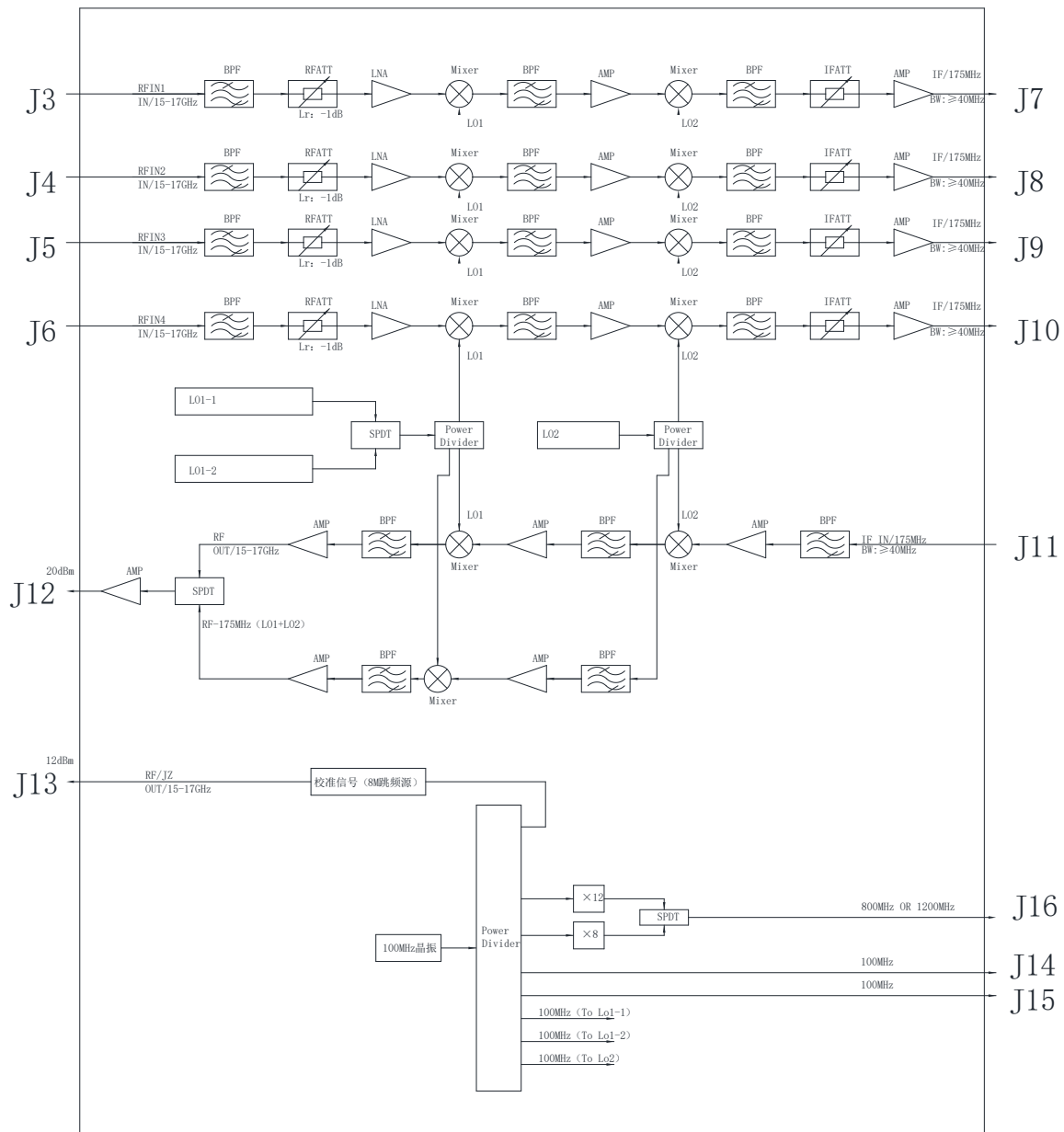


Features

This module features 1 transmit channel, 4 receive channels, 1 calibration channel, and 3 clock outputs. The built-in frequency synthesizer uses a ping-pong loop architecture to enable fast frequency hopping. It provides status monitoring functions including frequency synthesizer lock indication and transmit power amplifier detection indication.

Function Block Diagram



Specifications

Test Item		Symbol	Unit	Typ.
Clock Specifications	Output Power	P_o	dBm	5~10
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -155
	Spurious	R_{fs}	dBc	≤ -70
DDS Clock Signal	Output Power	P_o	dBm	5~10
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -125
	Spurious	R_{fs}	dBc	≤ -70
	Configuration Time	/	us	≤ 1
Calibration Signal	Output Power	P_o	dBm	≥ 12
	Frequency Hopping Time	t	us	≤ 100
	Spurious Suppression	R_{fs}	dBc	≥ 60
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -91
Receive Channel	Gain	G	dB	≥ 60
	Image Rejection	R_{IM}	dB	≥ 50
	Controllable Attenuation	A	dB	≥ 60 (Att. Step 1)
	Spurious Suppression	R_{fs}	dBc	≥ 60
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -91
	Output Frequency	f_o	MHz	175
	Maximum IF Output Power	P_{omax}	dBm	≤ 10
	Maximum Input Power	P_{imax}	dBm	-20
	Isolation Between Receive	ISO	dB	≥ 70
	Receive Channel	ΔA	dB	$\leq \pm 1$
	Receive Channel Phase	$\Delta \Phi$	° /度	$\leq \pm 20$
	Receive Desaturation Time	/	ns	≤ 150
	Receive Switching Time	/	ns	≤ 150
Transmit Excitation	Output Power	P_o	dBm	≥ 20
	Spurious Suppression	R_{fs}	dBc	≥ 60
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -91
External LO Output	Spurious Suppression	R_{fs}	dBc	≥ 60
	Phase @1kHz	$\mathcal{E}(f)$	dBc	≤ -91
	Frequency Hopping	/	MHz	8
	Frequency Hopping Time	t_p	us	≤ 2
	Output Power	P_o	dBm	≥ 20
Power Consumption		P	W	≤ 30

Product Render

The dimensions are 200mm × 220mm × 35mm.

