

Broadband SiP Frequency Source

Features

Input Frequency: 100MHz

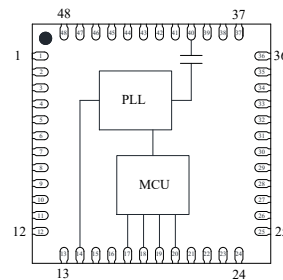
Input Power: (0 ± 3) dBm

Output Frequency: 0.1GHz~6.8GHz

Dimension: 6.0mm × 6.0mm × 1.0mm

Weight: $\leq 0.3g$

Function Block Diagram



Specifications ($T_A = -55^\circ\text{C} \sim 85^\circ\text{C}$, $V_{CC} = 3.3V$, REF Input Frequency: 100MHz, Input Power: 0dBm,

Input Phase noise: $-155\text{dBc/Hz}@1\text{kHz}$)

Parameter		Min	Typ	Max	Unit
Output Frequency		0.1		6.8	GHz
Frequency Step			5		MHz
Setting Time				20	μs
Output Power		0		7	dBm
Phase noise @6.8GHz	@100Hz			-80	dBc/Hz
	@1kHz			-96	
	@10kHz			-100	
	@100kHz			-100	
	@1MHz			-108	
	@10MHz			-140	
Spurs				-65	dBc
Current				200	mA

TYPICAL PERFORMANCE CHARACTERISTICS(Unless otherwise specified, $T_A = 25^\circ\text{C}$)

100MHz Phase noise



1GHz Phase noise

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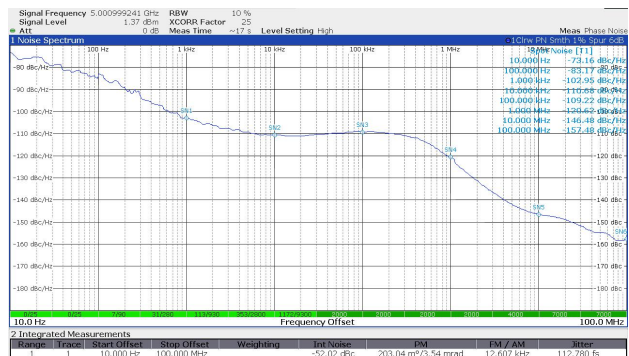
2.001GHz Phase noise



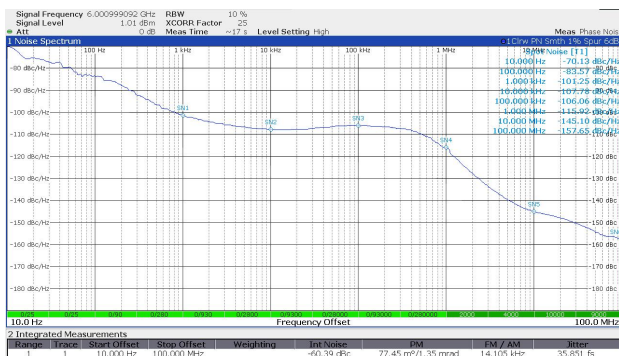
3.001GHz Phase noise



4.001GHz Phase noise



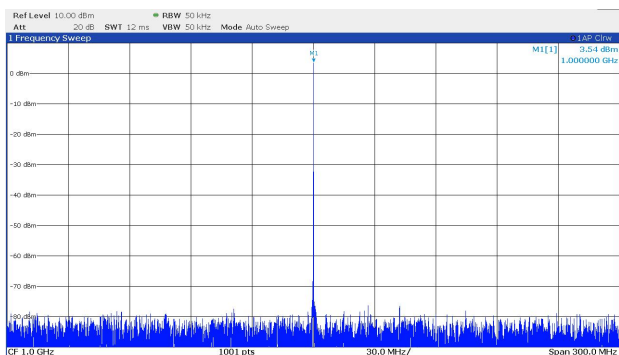
5.001GHz Phase noise



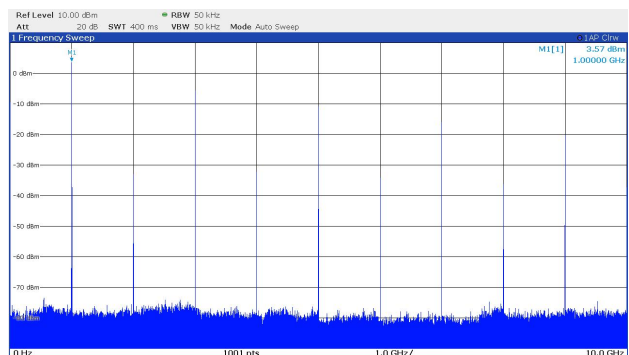
6.001GHz Phase noise



6.8GHz Phase noise

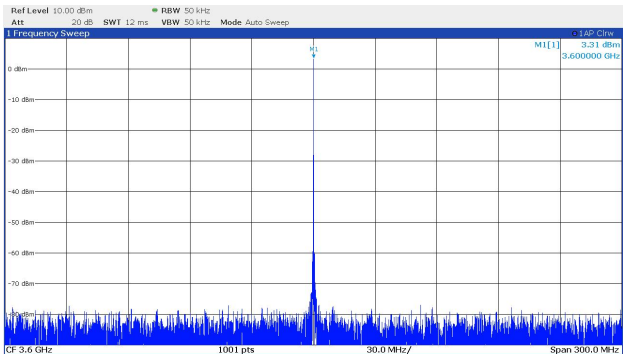


1GHz Spur (span=300MHz)

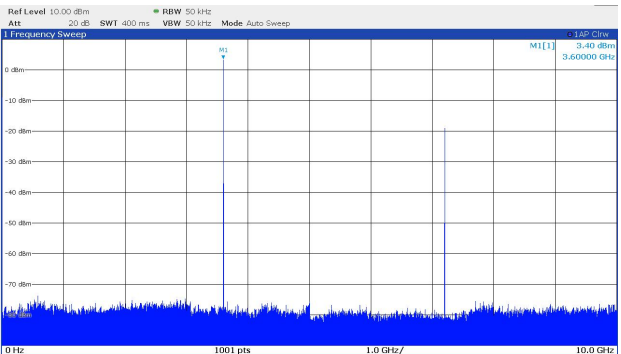


1GHz Spur (span=10GHz)

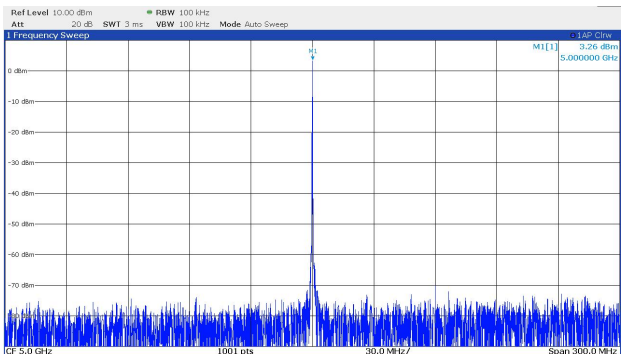
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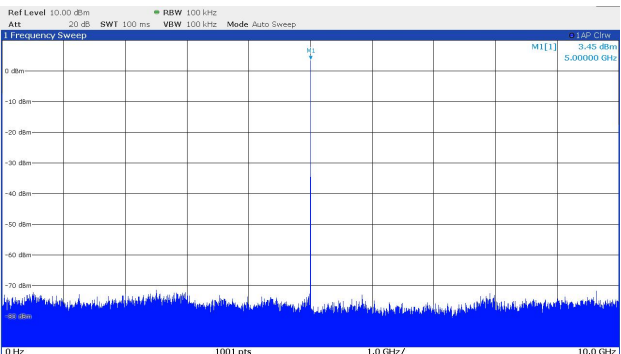
3.6GHz Spur (span=300MHz)



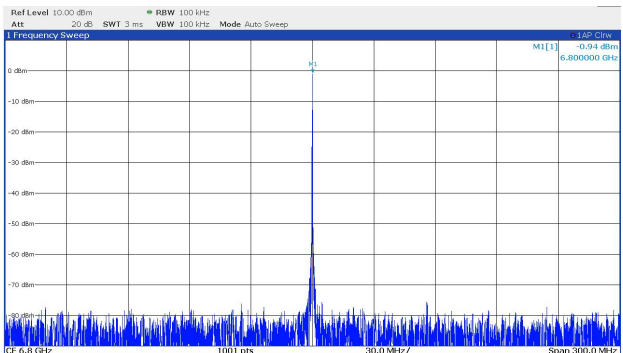
3.6GHz Spur (span=10GHz)



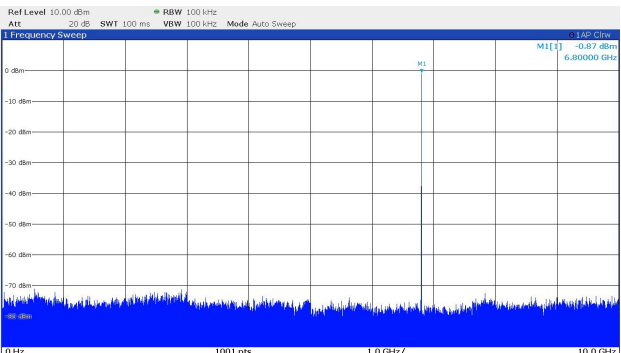
5GHz Spur (span=300MHz)



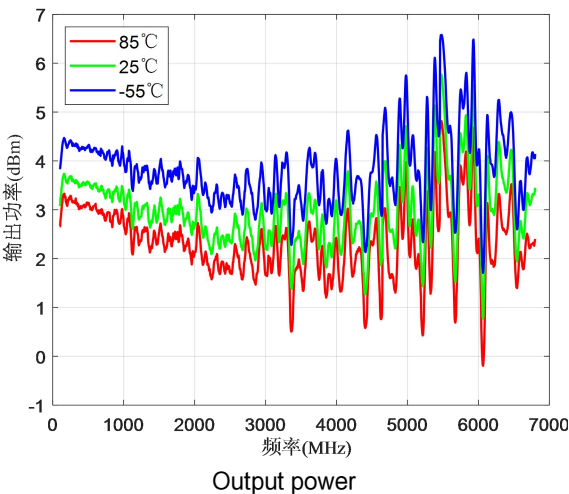
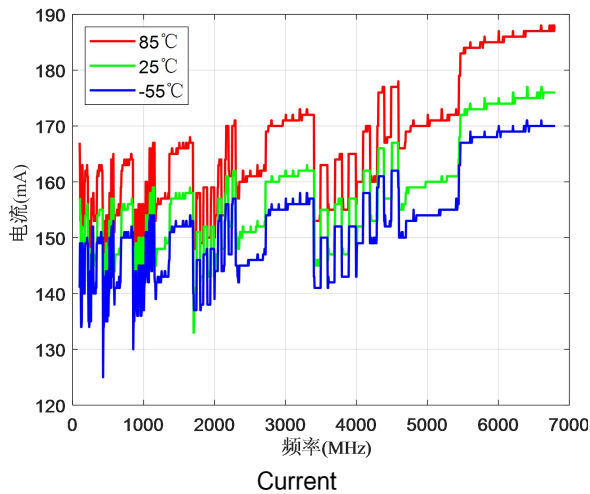
5GHz Spur (span=10GHz)



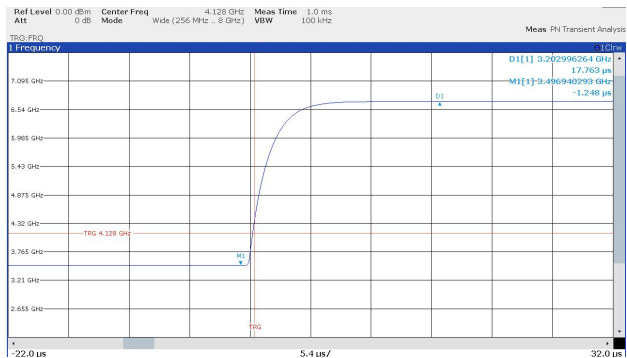
6.8GHz Spur (span=300MHz)



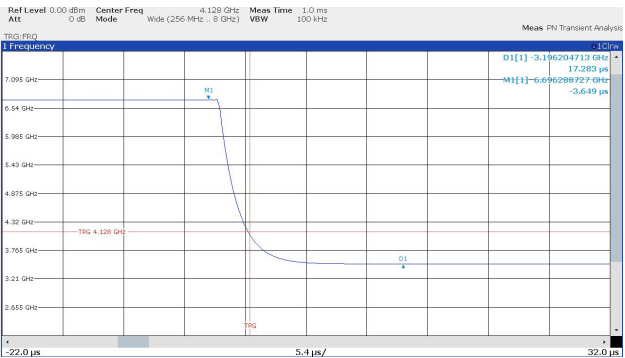
6.8GHz Spur (span=10GHz)



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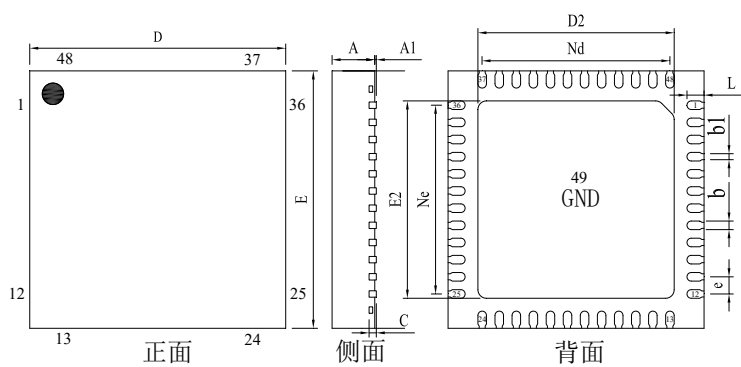


Frequency Settling Time (3.5GHz—6.7GHz)



Frequency Settling Time (6.7GHz —3.5GHz)

Outline



S	Dimensions(mm)			S	Dimensions(mm)		
	Min	Typ	Max		Min	Typ	Max
y				y			
m				m			
b				b			
ol				ol			
A	0.95	1.00	1.05	b	0.15	0.20	0.25
A	-	0.02	0.05	b	-	0.14	-
1				1			
c	-	0.203	-	e	-	0.40	-
N	-	4.40	-	N	-	4.40	-
e				d			
D	5.90	6.00	6.10	E	5.90	6.00	6.10
D	4.50	4.60	4.70	E	4.50	4.60	4.70
2				2			
L	0.35	0.40	0.45				

Pin Function

Pin No	Function	Pin Description
1	GND	Ground
2	VT	VCO tuning voltage input, leave unconnected
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	CP	Phase detector charge pump output
9	NC	No internal connection; may be ground or left floating
10	CAP4	Decompling pin, place a capacitor $\geq 1\mu$ F to ground

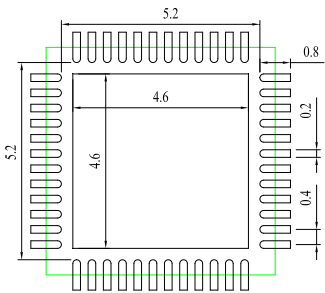
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		externally.CAP1–CAP4need to be inter connected on PCB
11	NC	No internal connection; may be ground or left floating
12	NC	No internal connection; may be ground or left floating
13	GND	Ground
14	REF	REF input
15	GND	Ground
16	CAP5	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.
17	LD	Lock Detect Output; output voltage: 2.7V~3.5V,under locked state, $\leq 0.5\text{V}$ under unlocked state
18	LE	SPI Chip Enable Input, 3.3V–LVTTL logic level
19	CLK	SPI Clock Input, 3.3V–LVTTL logic level
20	DAT	SPI Data Input, 3.3V–LVTTL logic level
21	IO	Spare general-purpose IO pin, keep floating
22	C2D	Firmware download port, can be routed out to a spare pad
23	GND	Ground
24	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
25	GND	Ground
26	C2K	Firmware download port, can be routed out to a spare pad
27	IO	Spare general-purpose IO pin, keep floating
28	IO	Spare general-purpose IO pin, keep floating
29	MD	Externally pulled up to 3.3Vvia a $5.1\text{k}\Omega$ resistor
30	IO	Spare general-purpose IO pin, keep floating
31	IO	Spare general-purpose IO pin, keep floating
32	NRST	MCU reset pin (3.3V–LVTTLlevel). Reset triggers at low level; the chip runs normally at high level. If this function is not used, mount an external RC delay circuit referring to the application schematic
33	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
34	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
35	NC	No internal connection; may be ground or left floating
36	CAP6	去耦端口, 至少 $2.2\mu\text{F}$ 电容到地
37	NC	No internal connection; may be ground or left floating
38	NC	No internal connection; may be ground or left floating
39	GND	Ground
40	RF	RF Output ,internal DC blocking capacitor
41	GND	Ground
42	CAP1	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB
43	GND	Ground
44	GND	Ground
45	CAP2	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB。

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46	GND	Ground
47	CAP3	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB
48	GND	Ground
49	GND	Ground

Recommended Footprint



Application note

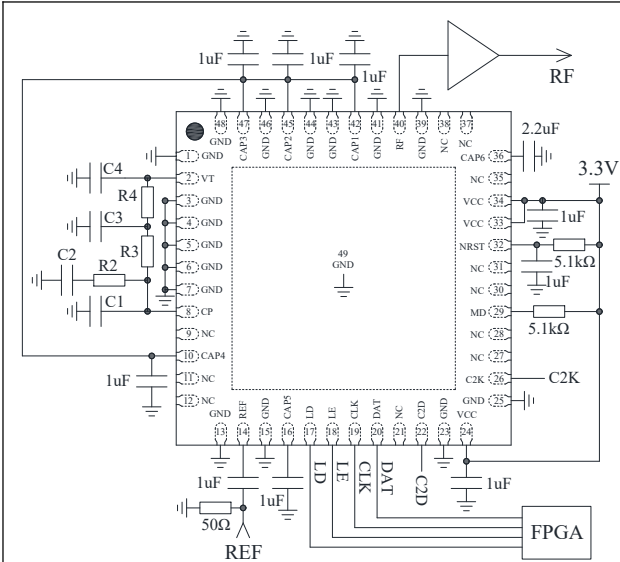


Figure 1 Application Circuit Diagram

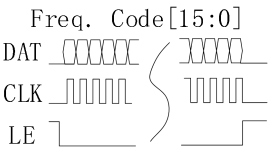


Figure 2 Timing Diagram

The 3.3V power supply of the circuit must pass through a low-noise LDO; otherwise, the phase noise of the output signal will be degraded. The communication control signals LD, LE, CLK and DAT shall be connected to the IO ports of FPGA. A 100 MHz reference signal is externally connected to the REF pin. The RF output contains no sub-harmonics and can be amplified directly to serve as the local oscillator signal.

The undetermined component values in Figure 1 are listed in the table below. All resistors and capacitors in the diagram can adopt 0402 package, and the rated voltage of all capacitors shall not be lower than 6.3 V.

C1	R2	C2	R3	C3	R4	C4
120pF	560 Ω	4700pF	0 Ω	Unmounted at initial state	820 Ω	10pF

The frequency hopping control of the circuit adopts 3-wire SPI synchronous serial input (LE, DAT, CLK), with a maximum serial clock frequency of 10 MHz.

The frequency code is composed of 2 bytes. When

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	transmitting codes, the high-order bits are sent first. After LE is pulled low for one clock cycle, the FPGA transmits DAT on the falling edge of CLK, while the frequency hopping source receives DAT on the rising edge of CLK. After the 16-bit data transmission is completed, LE is pulled high with a delay of one clock cycle. The decimal frequency code ranges from 0 to 1340, corresponding to output frequencies from 0.1 GHz to 6.8 GHz respectively. The code must be converted to hexadecimal before transmission. Example: For an output frequency of 6800 MHz, transmit the hex value 05 3C. The device outputs 3 GHz by default after power-up. If the input frequency code is outside the range of 0~1340, the output frequency remains unchanged.
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Absolute Maximum Ratings

VCC	+3.45V
Input Power	+10dBm
Storage Temperature	-55°C~100°C
Operating Temperature	-55°C~85°C
Reflow Soldering Peak Temperature	260°C
ESD Protection Classification Level(HBM)	Class 1C

Customization Notes

Internal firmware can be customized and modified to generate fixed-tone frequency sources or frequency-hopping sources with finer frequency step resolution.