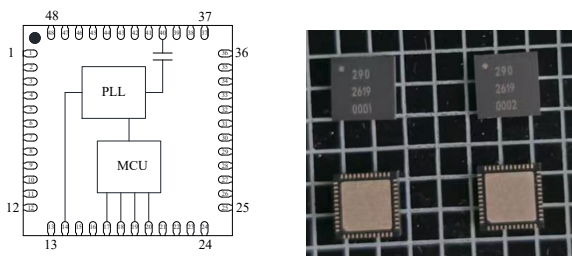


Fatures

Input Frequency:100MHz
Input Power: (0-7)dBm
Output Frequency:1GHz~20GHz
Dimension: 6.0mm × 6.0mm × 1.0mm
Weight: ≤0.3g

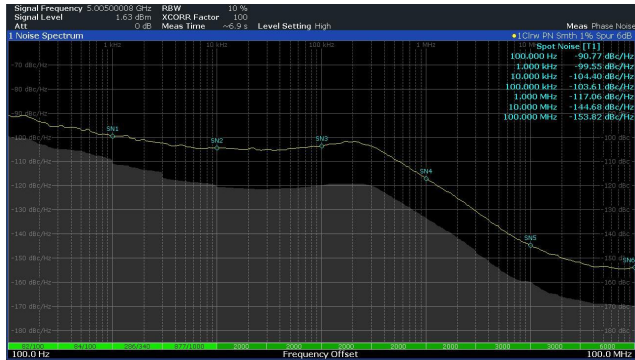
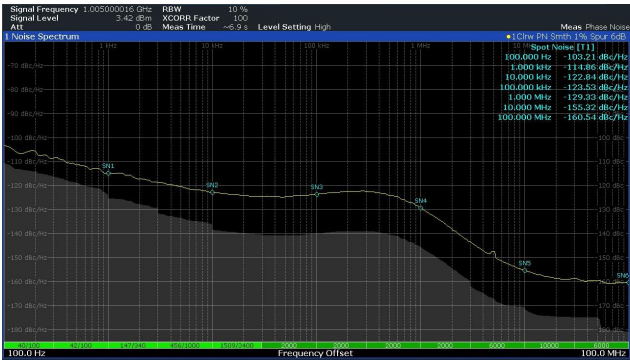
Function Block Diagram



Specifications($T_A=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}$, REF Input Frequency: 100MHz; Input Power: 5dBm; Input Phase noise: $-160\text{dBc/Hz}@1\text{kHz}$)

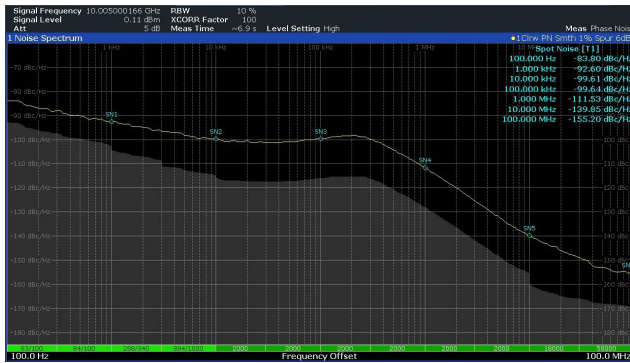
Parameter		Min	Typ	Max	Unit
Output Frequency		1		20	GHz
Frequency Step			5		MHz
Setting Time				20	μs
Output Power@20GHz		-8			dBm
Phase noise @20GHz	@100Hz			-75	dBc/Hz
	@1kHz			-87	
	@10kHz			-96	
	@100kHz			-98	
	@1MHz			-98	
	@10MHz			-125	
Spurs				-60	dBc
Current				450	mA

TYPICAL PERFORMANCE CHARACTERISTICS(Unless otherwise specified, $T_A=25^{\circ}\text{C}$)

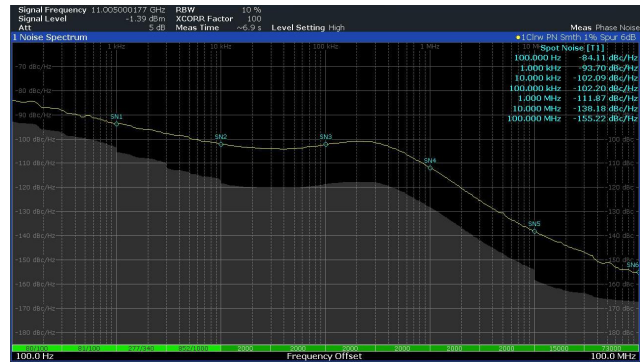


Broadband SiP Frequency Source

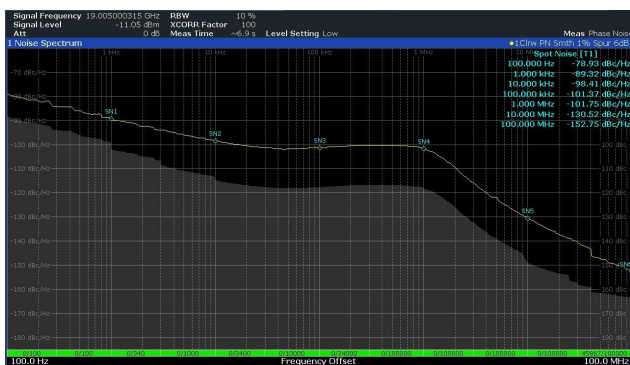
1.005GHz Phase noise



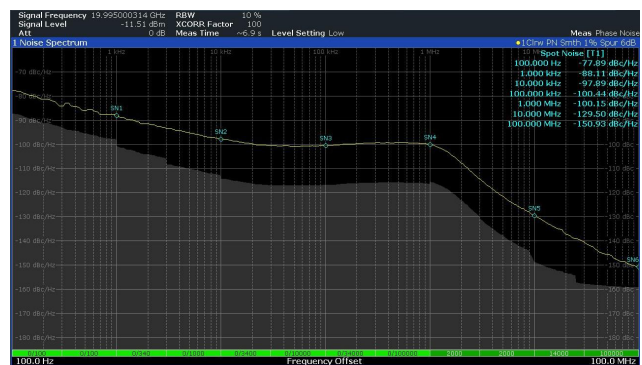
5.005GHz Phase noise



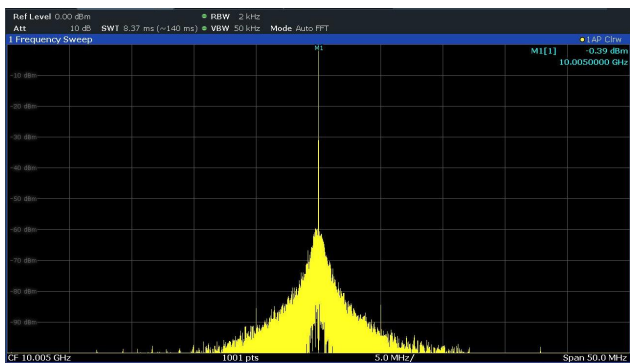
10.005GHz Phase noise



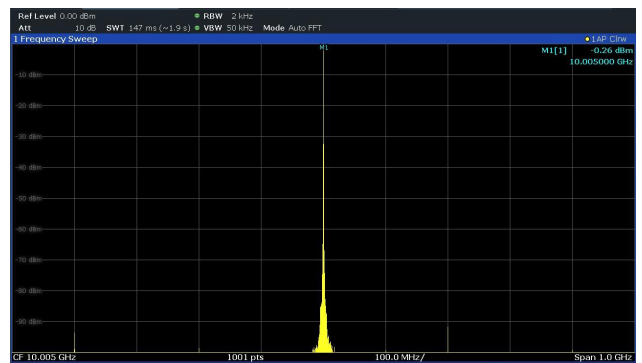
11.005GHz Phase noise



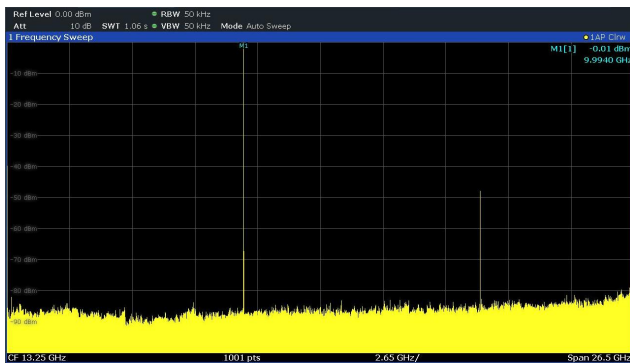
19.005GHz Phase noise



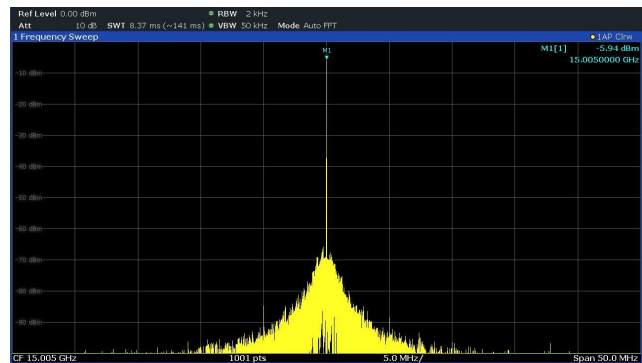
19.995GHz Phase noise



10.005GHz Spur (span=50MHz)



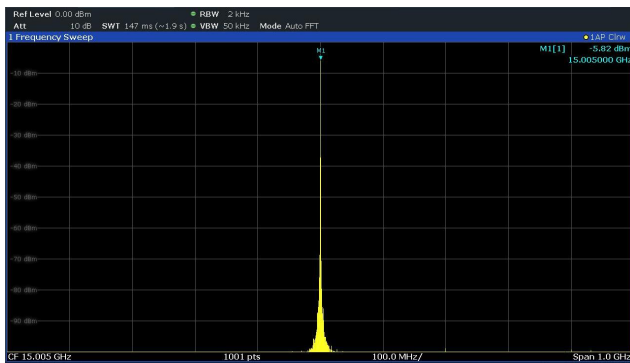
10.005GHz Spur (span=1GHz)



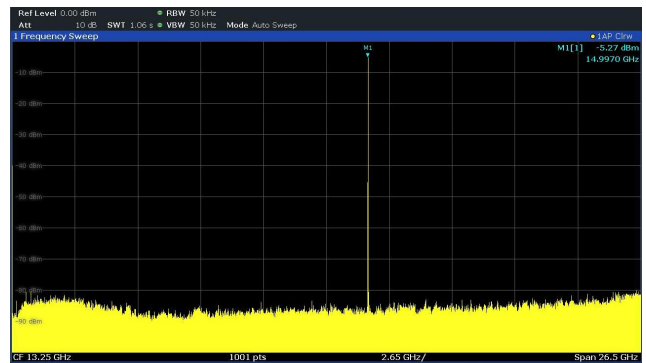
10.005GHz Spur (span=26.5GHz)

15.005GHz Spur (span=50MHz)

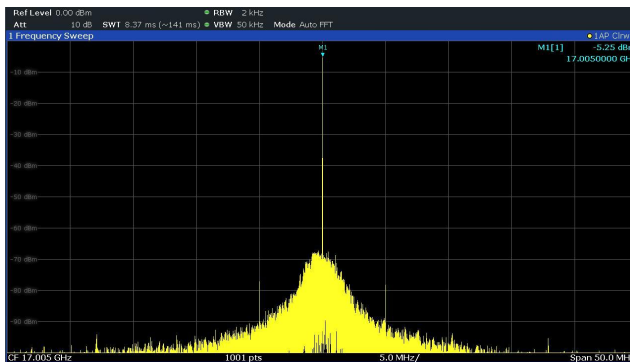
Broadband SiP Frequency Source



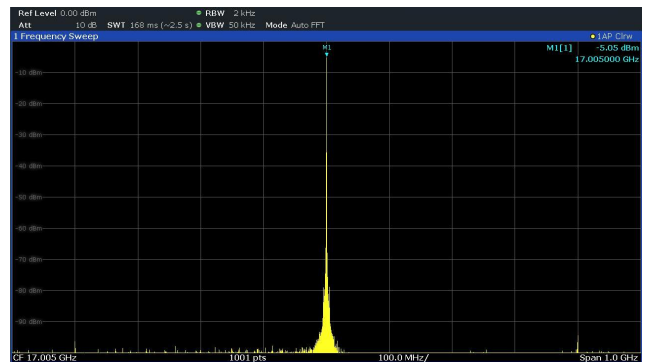
15.005GHz Spur (span=1GHz)



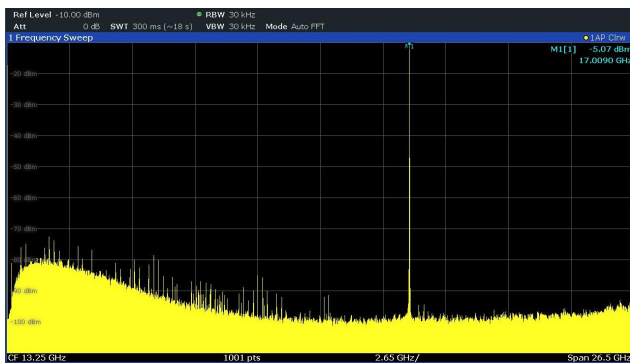
15.005GHz Spur (span=26.5GHz)



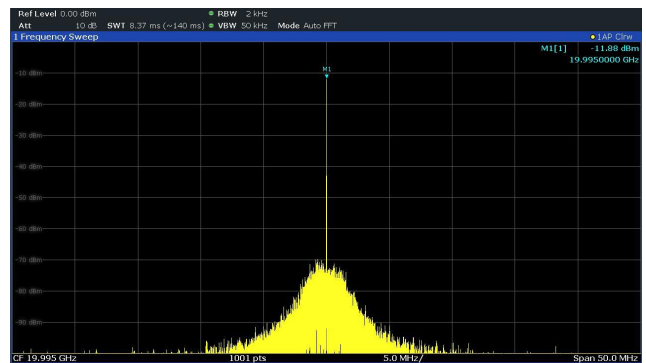
17.005GHz Spur (span=50MHz)



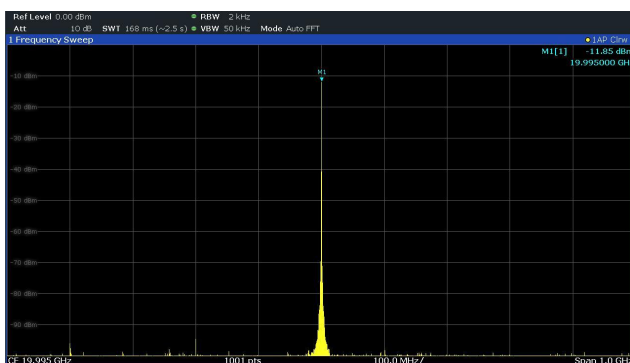
17.005GHz Spur (span=1GHz)



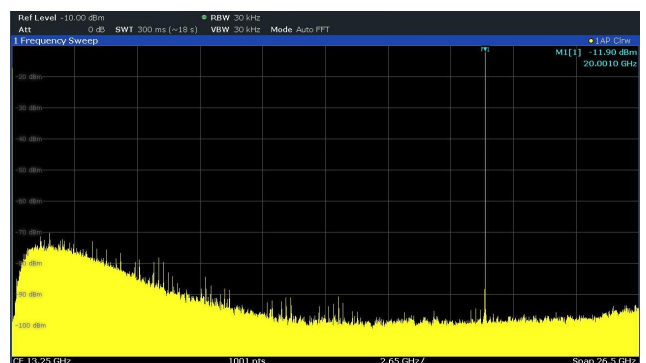
17.005GHz Spur (span=26.5GHz)



19.995GHz Spur (span=50MHz)

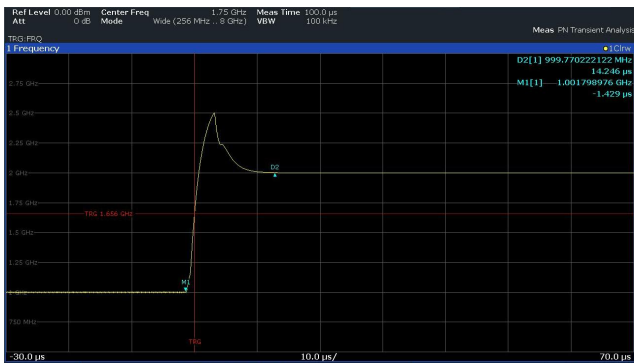


19.995GHz Spur (span=1GHz)

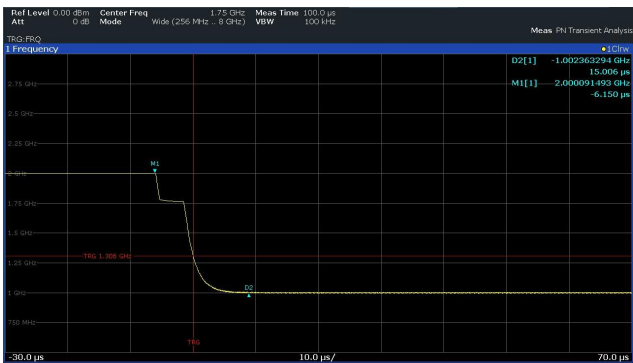


19.995GHz Spur (span=26.5GHz)

Broadband SiP Frequency Source

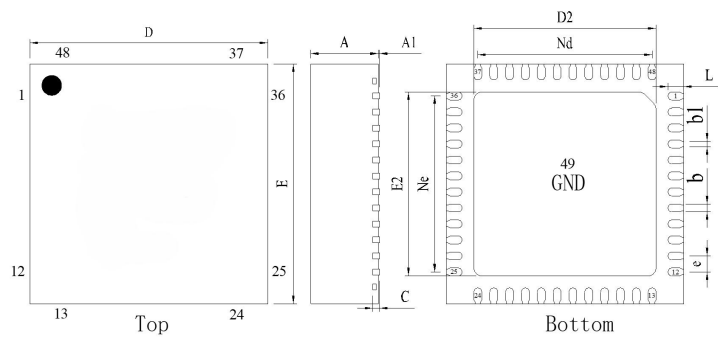


Frequency Settling Time(1GHz~2GHz)



Frequency Settling Time(2GHz~1GHz)

Outline



S	Dimensions(mm)			S	Dimensions(mm)		
	Min	Typ	Max		Min	Typ	Max
y				y			
m				m			
b				b			
ol				ol			
A	0.95	1.00	1.05	b	0.15	0.20	0.25
A	-	0.02	0.05	b	-	0.14	-
1				1			
c	-	0.203	-	e	-	0.40	-
N	-	4.40	-	N	-	4.40	-
e				d			
D	5.90	6.00	6.10	E	5.90	6.00	6.10
D	4.50	4.60	4.70	E	4.50	4.60	4.70
2				2			
L	0.35	0.40	0.45				

Pin Function

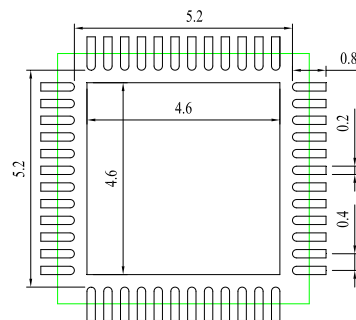
Pin No	Function	Pin Description
1	GND	Ground
2	Vt	VCO tuning voltage input, leave unconnected
3	GND	Ground
4	GND	Ground
5	GND	Ground
6	GND	Ground
7	GND	Ground
8	CP	Phase detector charge pump output
9	NC	No internal connection; may be ground or left floating
10	CAP4	Decompling pin, place a capacitor≥1uF to ground

		externally.CAP1–CAP4need to be inter connected on PCB
11	NC	No internal connection; may be ground or left floating
12	NC	No internal connection; may be ground or left floating
13	GND	Ground
14	REF	REF input
15	GND	Ground
16	CAP5	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.
17	LD	Lock Detect Output; output voltage: 2.7V~3.5V,under locked state, $\leq 0.5\text{V}$ under unlocked state
18	LE	SPI Chip Enable Input, 3.3V–LVTTL logic level
19	CLK	SPI Clock Input, 3.3V–LVTTL logic level
20	DAT	SPI Data Input, 3.3V–LVTTL logic level
21	IO	Spare general-purpose IO pin, keep floating
22	C2D	Firmware download port, can be routed out to a spare pad
23	GND	Ground
24	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
25	GND	Ground
26	C2K	Firmware download port, can be routed out to a spare pad
27	IO	Spare general-purpose IO pin, keep floating
28	IO	Spare general-purpose IO pin, keep floating
29	MD	Externally pulled up to 3.3Vvia a $5.1\text{k}\Omega$ resistor
30	IO	Spare general-purpose IO pin, keep floating
31	IO	Spare general-purpose IO pin, keep floating
32	NRST	MCU reset pin (3.3V–LVTTLlevel). Reset triggers at low level; the chip runs normally at high level. If this function is not used, mount an external RC delay circuit referring to the application schematic
33	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
34	VCC	3.3V power in; externally mount a capacitor of at least $1\mu\text{F}$ to ground
35	NC	No internal connection; may be ground or left floating
36	NC	No internal connection; may be ground or left floating
37	NC	No internal connection; may be ground or left floating
38	NC	No internal connection; may be ground or left floating
39	GND	Ground
40	RF	RF Output
41	GND	Ground
42	CAP1	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB
43	GND	Ground
44	GND	Ground
45	CAP2	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB

Broadband SiP Frequency Source

46	GND	Ground
47	CAP3	Decompling pin, place a capacitor $\geq 1\mu\text{F}$ to ground externally.CAP1–CAP4need to be inter connected on PCB
48	GND	Ground
49	GND	Ground

Recommended Footprint



Application note

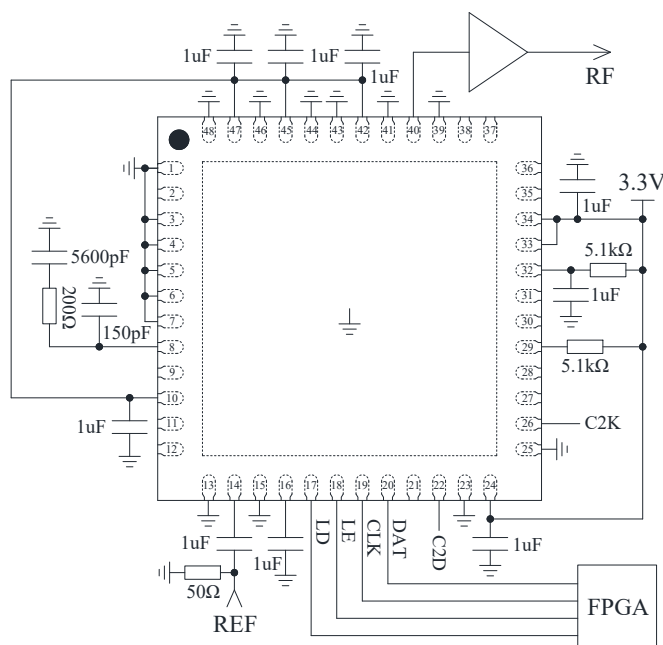


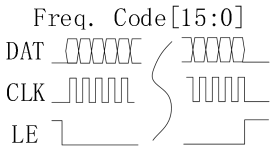
Figure1 Application Circuit Schematic

The circuit requires a +3.3V power supply routed through a low-noise LDO; otherwise, the phase noise of the output signal may degrade. Control signals LD, LE, CLK and DAT are interfaced to FPGA GPIO ports. A 100MHz reference clock shall be connected to the REF pin. The RF output features spurious-free spectrum and can be amplified directly to serve as the local oscillator signal. For RF operating frequencies above 16GHz, a high-pass filter is recommended for spurious suppression across the 0-5GHz band (built-in spurious suppression performance: -60 dBc).

Frequency tuning adopts 3-wire SPI synchronous serial interface (LE, DAT, CLK), with a maximum serial clock rate of 10MHz.

The 16-bit frequency word is transmitted with high-order bits sent first. Pull LE low for one clock cycle, the FPGA transmits DAT data on the falling edge of CLK; the frequency synthesizer latches DAT on the rising edge of CLK. After all 16-bit data transmission completes, assert LE high with a single clock cycle delay.

Broadband SiP Frequency Source

Freq. Code[15:0]  Figure2 Timing Diagram	Decimal frequency codes ranging from 0 to 3800 correspond to 1GHz~20GHz output frequencies respectively. Convert decimal tuning values to hexadecimal prior to transmission. The device powers up with a default 10GHz RF output. When a code outside the 0~3800 range is loaded, the synthesizer retains the existing operating frequency.
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Absolute Maximum Ratings

VCC	+3.45V
Input Power	+10dBm
Operating Temperature	-55°C~100°C
Storage Temperature	-40°C~85°C
Reflow Soldering Peak Temperature	260°C
ESD Protection Classification Level(HBM)	Class 1C

Customization Notes

Internal firmware can be customized and modified to generate fixed-tone frequency sources or frequency-hopping sources with finer frequency step resolution.